

What is claimed is:

1. A rate generator for generating a plurality of frequencies comprising:

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an oscillator comprising:

a phase accumulator for storing an accumulated phase value;

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a phase increment register for storing a phase increment value; and

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an adder, coupled to said phase accumulator and said phase increment register, for summing said phase increment value and the accumulated phase value to provide a sum to said phase accumulator, said adder for generating a pulse at a frequency each time the sum reaches a pre-determined value; and

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a controller, coupled to said oscillator, for time sharing said phase accumulator, phase increment register and said adder to operate said oscillator as a plurality of oscillators to produce a plurality of frequencies.

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2. The rate generator of claim 1 further comprising a plurality of oscillators and controllers.

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3. The rate generator of claim 1 wherein said phase accumulator is an accumulated phase value storage for storing a plurality of accumulated phase values, said phase increment register is a phase increment value storage for storing a plurality of phase increment values, and said controller is a memory address generator for addressing said phase accumulator value storage and said phase increment value storage to timely apply said values to said adder.

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4. The rate generator of claim 3 wherein the accumulated phase value storage stores 64 accumulated phase values and said phase increment value storage stores 64 phase increment values.

5. The rate controller of claim 1 wherein said plurality of oscillators is 64.

5 6. The rate controller of claim 1 wherein said plurality of frequencies for a write enable signal for a memory that stores stream identifiers.

7. A rate generator for generating a plurality of stream  
10 identifiers for a selected number of users, the rate generator comprising a plurality of parallel groups, each group comprising:

an address generator for generating a plurality of  
15 identifiers;

a phase increment source for generating a plurality of phase increments associated the plurality of identifiers;

20 a phase accumulator module having a plurality of phase accumulators, said phase accumulator module for receiving an accumulated phase value and providing the phase value of one of the phase accumulators during a frequency cycle;

25 a phase increment module having a plurality of phase increment registers pre-loaded with a phase increment value, said phase increment module for providing an output of one of the phase increment registers during the frequency cycle;

30 an adder, coupled to said phase accumulator module and said phase increment module, for summing the phase increment value and the output of said phase accumulator module and providing the sum to said phase accumulator module, said adder for generating a pulse each time the sum reaches a  
35 pre-determined value; and

sequencing means, coupled to said address generator and said adder for pipelining the plurality of stream

identifiers and for outputting one stream identifier each time said adder generates the pulse.

8. The rate generator of claim 7 wherein the plurality of  
5 identifiers comprise user identifier addresses in a video on demand system.

9. The rate generator of claim 7 wherein said sequencing means comprises a first-in-first-out (FIFO) queue.

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10. A method for deriving a rate generator architecture having a plurality of accumulators, the rate generator architecture for a selected number of users, the method  
15 comprising:

calculating a number of bits required of each accumulator;

20 calculating a number of accumulators to sequentially implement; and

calculating a number of groups from the calculated number of accumulators and the selected number of users.

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11. The method of claim 10, wherein the method further comprises the steps of:

providing an adder within each group; and

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providing one phase increment register for each accumulator.

12. The method of claim 10, wherein said bit calculating  
35 step comprises the steps of:

determining a maximum sampling rate for transmitting data packets

determining an error frequency associated with a tolerable packet error; and

5        calculating the numbers of bits required from the maximum sampling rate and the error frequency.

13. The method of claim 12, wherein said maximum sampling rate determining step comprises the steps of:

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      providing a number of bits per packet;

      providing a maximum bit rate;

15        determining a maximum packet frequency from the maximum bit rate and the number of bits per packet;

      selecting a number of samples per packet; and

20        determining a maximum sampling frequency from the number of samples per packet and the maximum packet frequency.

14. The method of claim 10 wherein said accumulator  
25        calculating step comprises the steps of:

      adjusting the sampling frequency;

      selecting a clock frequency; and

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      calculating the number of accumulator bits from the adjusted sampling frequency and the clock frequency.